CLAIM AMENDMENTS

Please amend claims 6, 12 and 21. Please add claims 25-27. Listed below are the claims as originally filed and their current status.

IN THE CLAIMS:

Claims 1-5 (Cancelled).

6. (Amended) An electrical semiconductor device comprising:

a high resistivity layer of one conductivity type and having opposing first and second surfaces;

a layer of relatively low resistivity material of a conductivity type opposite to the one conductivity type and having a surface substantially contiguous to the first surface of the high resistivity layer; ~~and~~

a dopant region of relatively low resistivity material of the one conductivity type having a surface substantially contiguous to the second surface of the high resistivity layer;

a substantially centrally defined well in said high resistivity layer, said well reducing ~~wherein the second surface has a well that reduces~~ the thickness in a portion of the high resistivity layer, thus reducing an electric field in said portion of the semiconductor device; and

an edge termination defined in part by a moat.

7. (Previously Presented) The device of claim 6 wherein the second surface is etched, and the dopant region is diffused into the second surface of the high resistivity layer.

8. (Previously Presented) The device of claim 6 wherein the second surface well is etched, and the dopant region is epitaxially grown onto the second surface of the high resistivity layer.

9. (Previously Presented) The device of claim 6 wherein a silicon oxide mask is applied to the first surface of the layer of relatively low resistivity and the dopant region is diffused through the silicon oxide mask and into the second surface of the layer of relatively low resistivity.

10. (Previously Presented) The device of claim 6 wherein the high resistivity layer includes a stress-relieving dopant.

11. (Original) The device of claim 10 wherein the stress-relieving dopant is germanium.

12. (Amended) An electrical semiconductor device comprising:

a high resistivity layer of one conductivity type and having opposing first and second surfaces, the high resistivity layer further having a dopant material permeated throughout the layer;

a layer of relatively low resistivity material of a conductivity type opposite to the one conductivity type and having a surface substantially contiguous to the first surface of the high resistivity layer; and

a region of relatively low resistivity material of the one conductivity type having a surface substantially contiguous to the second surface of the high resistivity layer;

wherein the second surface of the high resistivity layer has a substantially centrally located well that reduces the thickness in a portion of the high resistivity layer, thus reducing an electric field in said portion of the electrical semiconductor device and wherein the electrical semiconductor device has an edge termination defined in part by a moat.

13. (Previously Presented) The device of claim 12 wherein the region contains a stress-relieving dopant.

14. (Original) The device of claim 13 wherein the stress-relieving dopant is germanium.

15. (Previously Presented) The device of claim 12 wherein a silicon oxide mask is applied to the second surface of the high resistivity layer and the region is diffused through the silicon oxide mask and into the second surface of the high resistivity layer.

16. (Withdrawn) A method for fabricating an electrical semiconductor device comprising:

selecting a substrate of relatively low conductive material of one conductivity type, the substrate having opposing first and second surfaces;

etching the first surface of the substrate;

diffusing a region of high conductivity material of the one conductivity type into the first surface of the substrate; and

growing an epitaxial layer of high conductivity material onto the second surface of the substrate, the epitaxial layer having a conductivity type opposite to the one conductivity type.

17. (Withdrawn) A method for fabricating an electrical semiconductor device comprising:

preparing a substrate of relatively low conductivity material of one conductivity type, the substrate having opposing first and second surfaces;

etching the first surface of the substrate;

growing a first epitaxial layer of high conductivity material of the one conductivity type onto the first surface of the substrate; and

growing a second epitaxial layer of high conductivity material onto the second surface of the substrate, the second epitaxial layer having a conductivity type opposite to the one conductivity type.

18. (Withdrawn) A method for fabricating an electrical semiconductor device comprising:

selecting a substrate of relatively high conductivity material of one conductivity type, the substrate having a first surface;

growing an epitaxial layer onto the first surface of the substrate, the epitaxial layer having opposing first and second surfaces, with the first epitaxial surface being substantially contiguous to the first surface of the substrate, and being of a low conductivity material of a conductivity type opposite to the one conductivity type;

introducing a dopant material to the epitaxial layer;

applying a silicon oxide layer to the second epitaxial surface;

creating a silicon oxide mask by etching portions of the silicon oxide layer to expose portions of the second epitaxial surface; and

diffusing a high conductivity layer through the mask and into the second epitaxial layer, the diffused layer being of a conductivity type opposite to the one conductivity type

19. (Withdrawn) The device of claim 18 wherein the dopant material is a stress-relieving dopant material.

20. (Withdrawn) The device of claim 18 wherein the stress-relieving dopant material is germanium.

21. (Amended) An electrical semiconductor device comprising:

a first layer of relatively high resistivity material of one conductivity type having opposing first and second surfaces;

a second layer of relatively low resistivity material of a conductivity type opposite to the one conductivity type and having one surface substantially contiguous to the first surface of the substrate;

a region of relatively low resistivity material of the one conductivity type and having one surface substantially contiguous to the second surface of the substrate; ~~and~~

a substantially centrally located well formed in the first layer such that the distance between the region and the second layer is reduced at the location of the well, said well able to receive a conductive layer; and

an edge termination defined in part by a moat.

22. (Cancelled).

23. (Cancelled).

24. (Previously Presented) The device of claim 15 wherein the second surface of the high resistivity layer receives a lesser amount of diffused material to form said to reduce said resulting electric field.

25. (New) The device of claim 6, wherein said well has a diffused dopant region.

26. (New) The device of claim 6, wherein said well receives a conductive layer.

27. (New) The device of claim 6, wherein said well is bounded by a bottom surface and a side surface, the side surface defining a depth distance between said first surface and said bottom surface and wherein said distance between said second surface and said bottom surface is less than the distance between said first surface and said second surface.